ABSTRACT OF THE DISCLOSURE

There is provided a phase locked loop circuit capable of obtaining an output frequency having no fraction even in case a reference signal has a rounded frequency (e.g., 10 MHz).

The phase locked loop circuit uses a fractional frequency divider, comprises: a first PLL stage for controlling the output frequency of a first voltage-controlled oscillator with a deviation, which is obtained by dividing the frequency of the output of the first voltage-controlled oscillator by a first fractional frequency divider and by comparing the frequency-divided output with a reference frequency, through a low-pass filter; and a second fractional frequency divider for dividing the frequency of the output of the first PLL stage and for inputting the frequency-divided output as a reference frequency signal of a second PLL stage. The output signal of a second voltage-controlled oscillator of the second PLL stage is extracted.